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PATENT
#15 (1/10/03)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Internal application of:

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APR 03 2003

Technology Center 2100

Sharad Kapur, *et al.*

Serial No.: 09/427,238

Filed: October 26, 1999

For: SYSTEM AND METHOD FOR DETERMINING CAPACITANCE
FOR LARGE-SCALE INTEGRATED CIRCUITS

Group No.: 2123

Examiner: Eduardo Garcia-Otero

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Commissioner for Patents
Washington, D. C. 20231

<p>I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on 03/27/2003 (Date)</p> <p><u>Sharad Kapur</u> (Printed or typed name of person signing the certificate)</p> <p><u>Sharad Kapur</u> (Signature of the person signing the certificate)</p>

Sir:

"REQUEST FOR APPROVAL OF PROPOSED DRAWING CORRECTION"

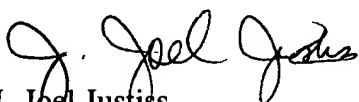
FIGURES 1 and 2B have been modified to provide a better understanding of the subject matter. Since these aspects of the present invention were submitted in the application as originally filed, the corrected drawings do not constitute new matter. The Applicants hereby submit a proposed drawing correction for the appropriate figures in which the proposed corrections are marked in red ink. Accordingly, approval of each of the proposed drawing corrections is respectfully requested.

10/12/03
Eg
CORRECTIONS APPROVED

In the event that each proposed drawing correction is not approved in its entirety, the undersigned will attend to the correction of these drawings in the manner specified by the Examiner.

Respectfully submitted,

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Date: 3/27/03

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